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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Celii et al.

Art Unit: 1765

Serial No.: 09/599,718

Examiner: Brown, C.

Filing Date: 08/22/00

Docket No.: TI-29276

Title: PROCESS FLOW FOR DUAL DAMESCENE INTERCONNECT  
STRUCTURESAmendment under 37 CFR 1.115Assistant Commissioner of Patents  
Washington, DC 20231OFFICIAL  
FAX RECEIVED  
JUL 29 2002  
GROUP 1700

Dear Sir:

The following amendments and remarks are offered in response to the Examiner's Office Action dated 02/28/02. They are respectfully submitted as a full and complete response to that Action.

Please amend the above-referenced application as follows:

In the Claims:

Amend Claim 1 to read as follows:

- Sho  
A1
1. (amended) A method of fabricating an integrated circuit, comprising the steps of:
- forming an interlevel dielectric layer over a semiconductor body;
  - forming an intrametal dielectric layer over said interlevel dielectric layer;
  - forming a hardmask over said intrametal dielectric layer;
  - forming a via pattern over said hardmask;
  - selectively etching a via through said hardmask;
  - extending said via by selectively etching said intrametal dielectric layer;

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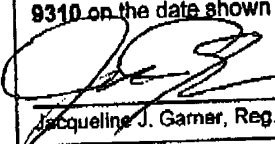
Serial No.: 09/599,718

Examiner: Brown, C.

Filing Date: 06/22/00

Docket No.: TI-29276

Title: PROCESS FLOW FOR DUAL DAMESCE INTERCONNECT  
STRUCTURES

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I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9310 on the date shown below:	
	July 29, 2002
Jacqueline J. Garner, Reg. No. 36,144	Date

## FACSIMILE COVER SHEET

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<input type="checkbox"/> NEW APPLICATION	<input checked="" type="checkbox"/> EOT 2mth (3 Pages)
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<input type="checkbox"/> CONTINUATION APP'N (# Pages)	
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NAME OF INVENTOR(S): Celii	
TITLE OF INVENTION: Process Flow for Dual Damescene Interconnect	
TI FILE NO.: TI-29276	DEPOSIT ACCT. NO.: 20-0668
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